side surface of said trench, wherein the transistor comprises a plurality of said source regions and outer periphery of each said source regions is exposed at a side of upper part of said trench; and

a metal film formed on a surface of said drain layer opposite to said conductive region to establish Schottky contact with said drain layer.

19. A transistor according to claim 18, wherein each of said source regions is annular when viewed from a direction parallel to said side surface of said trench.

REMARKS

Claims 1, 2, 6, 7, 10 and 11 have been amended, and claims 16 - 19 have been added in order to more particularly point out, and distinctly claim the subject matter to which the applicants regard as their invention. It is believed that this Amendment is fully responsive to the Office Action dated April 4, 2002.

This Amendment is timely filed on July 5, 2002, July 4, 2002 being a federal holiday.

Claims 1 - 11 are currently pending in this patent application, claims 12 - 15 having been withdrawn for being non-elected claims.

Claims 1 - 11 stand rejected under 35 USC §112, second paragraph, for the specific reasons set forth on page 3 of the outstanding Action. The applicants respectfully request reconsideration of this rejection.

As indicated above, claims 1, 2, 6, 7, 10 and 11 have been amended in order to more particularly point out, and distinctly claim the subject matter to which the applicants regard as their invention, and in order to correct certain informalities therein, including those which have been pointed out by the Examiner.

Accordingly, the withdrawal of the outstanding indefiniteness rejection under 35 USC §112, second paragraph, is in order, and is therefore respectfully solicited.

As to the merits of this case, claims 1 - 11 stand rejected under 35 USC §102(e) as being anticipated by Baliga (U.S. Patent No. 5,998,833). The applicants respectfully request reconsideration of this rejection.

A significant structural arrangement of the applicants' power MOSFET 1 is the source electrode film 29 and the source region 27 in each cell 3 being in direct contact with each other on: (1) a top surface 51 of the semiconductor substrate 5, and (2) an inner circumferential surface 52 of the trench 18, and are electrically connected to each other. Consequently, the area of the source

regions 27 exposed on the inner side surface 52 of the trench 18 can be increased; thereby, increasing the contact area between the source regions 27 and the source electrode film 29.

By doing so, there is no need to increase the size of the source regions 27 along the substrate top surface 51; thereby, reducing the area occupied by the source regions, and the size of the device.[1]

In the Examiner's reliance of the Baliga patent, the Examiner specifically states the following with respect to the last clause of independent claim 1:

> a source electrode film provided in contact with at least the source region exposed on the inner circumferential surface of the trench and electrically insulated from the gate electrode material (fig. 2 # 118 col. 3 lines 45-50 and fig. 3 # 128b col. 6 lines 51-56).[2]

(See, also, lines 1 - 4, page 7 of the outstanding Action with respect to the Examiner's comments regarding the last clause of independent claim 11.) However, in reviewing the above-cited portions of the Baliga patent, Baliga is not concerned with the increase in the contact area between a source region and a source electrode film by increasing the area of the source region exposed on the inner circumferential or side surface of the trench. Instead, Baliga, in lines 45 - 50, column 3, is merely concerned with the control of the various thicknesses T1, T2 of the gate insulating region 124, as illustrated in Baliga's Figure 2 in order to "inhibit the occurrence of high electric fields at the bottom of the trench and to provide a substantially uniform potential gradient along the trench sidewalls

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[1]See, for example, line 22, page 20 through line 14, page 21 of the applicants' specification.

[2]See, 10 - 13, page 5 of the outstanding Action.

120a," and "to maintain a threshold voltage of the device at about 2-3 volts."[3]

As to Baliga's lines 51 - 56, column 6, and Figure 3, the teachings are limited to a discussion of a source electrode 128b and a drain electrode 130 extending in parallel across first and second faces of gate electrode/source electrode insulating region 125.

In view of the above, the applicants respectfully submit that not all of the claimed elements, as now set forth in each of independent claims 1 and 11, are found in exactly the same situation and united in the same way to perform the identical function in Baliga's device. Thus, there can be no anticipation of the applicants' claimed invention, as now set forth in each of independent claims 1 and 11, under 35 USC §102(e) based on Baliga.

Moreover, claims 2 - 10 depend on independent claim 1, and further limit the scope of independent claim 1. Thus, at least for the reasons set forth above with respect to independent claim 1, claims 2 - 10 should now be similarly allowable.

In view of the above, the withdrawal of the outstanding anticipation rejection under 35 USC §102(e) based on Baliga (U.S. Patent No. 5,998,833) is in order, and is therefore respectfully solicited.

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[3]See, lines 38 - 49, column 3 in Baliga.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact the applicants' undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

In the event that this paper is not timely filed, the applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully Submitted,

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PATENT TRADEMARK OFFICE

Enclosures: Version with markings to show changes made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE 09/660,439

IN THE CLAIMS:

Please amend claims 1, 2, 6, 7, 10 and 11 as follows:

1. (Amended) A transistor comprising;

a semiconductor substrate having a semiconductor layer, a drain layer of a first conductivity type provided on said semiconductor layer and [an oppositely] a conductive region of a second conductivity type [provided on said drain layer] formed by diffusing an impurity of the second conductivity type from a surface of said drain layer;

a trench provided such that it extends from a surface of said [oppositely] conductive region to said drain layer;

a source region of the first conductivity type provided [in] inner surface of said [oppositely] conductive region and exposed on [an inner circumferential] side surface of said trench;

a gate insulating film provided on [the inner circumferential] the side surface [and inner bottom surface] of said trench [such that it reaches to said drain layer, said oppositely conductive region and said source region], an upper part of the gate insulating film being in contact with a lower part of said source region, a bottom part being in contact with an upper part of said drain layer, and a middle part being in contact with conductive region;

a gate electrode material provided in [tight] contact with said gate insulating film in said trench;

a source of electrode film provided in contact with at least said source region exposed at least on the [inner circumferential] side surface of said trench and electrically insulated from said gate electrode material, said source region being substantially square when viewed from a direction parallel to said side surface of said trench.

2. (Amended) A transistor according to Claim 1, further comprising a drain electrode film formed on a surface of said semiconductor layer located opposite [to] said drain layer.

6. (Amended) A transistor according to Claim 4, wherein said insulating material has a thickness [between] of at least 0.01 μm and at most 1.0 μm.

7. (Amended) A transistor according to Claim 5, wherein said insulating material has a thickness [between] of at least 0.01 μm and at most 1.0 μm.

10. (Amended) A transistor according to Claim 1, wherein said semiconductor layer is of the second conductivity type [as opposed to said drain layer].

11. (Amended) A transistor comprising:

a semiconductor substrate having a drain layer of a first conductivity type and [an oppositely] a conductive region of a second conductivity type [provided on said drain layer] formed by diffusing an impurity of the second conductivity type from a surface of said drain

layer;

a trench provided such that it extends from a surface of said [oppositely] conductive region to said drain layer;

a source region of the first conductivity type provided ~~in~~ inner surface of said [oppositely] conductive region and exposed on [an inner circumferential] side surface of said trench;

a gate insulating film provided on the [inner circumferential] side surface[and inner bottom surface] of said trench [such that it reaches to said drain layer, said oppositely conductive region and said source region], an upper part of the gate insulating film being in contact with a lower part of said source region, a bottom part being in contact with an upper part of said drain layer, and a middle part being in contact with said conductive region;

a gate electrode material provided in [tight] contact with said gate insulating film in said trench;

a source electrode film provided in contact with [at least] said source region exposed at least on the [inner circumferential] side surface of said trench and electrically insulated from said gate electrode material,

said source region being substantially square when viewed from a direction parallel to said side surface of said trench; and

a metal film formed on a surface of said drain layer opposite to said [oppositely] conductive region to establish Schottky contact with said drain layer.

Please add claims 16 - 19 as follows:

16. A transistor comprising:

a semiconductor substrate having a semiconductor layer, a drain layer of a first conductivity type formed by diffusing an impurity of the second conductivity type from a surface of said drain layer;

a trench provided such that it extends from a surface of said conductive region to said drain layer;

a source region of the first conductivity type provided inner surface of said conductive region and exposed on a side surface of said trench;

a gate insulating film provided on the side surface of said trench, an upper part of the gate insulating film being in contact with a lower part of said source region, a bottom part being in contact with an upper part of said drain layer, and a middle part being in contact with said conductive region;

a gate electrode material provided in contact with said gate insulating film in said trench;

a source electrode film provided in contact with said source region exposed at least on the side surface of said trench and electrically insulated from said gate electrode material,

wherein the transistor comprises a plurality of said source regions and outer periphery of each of said source regions is exposed at a side of upper part of said trench.

17. A transistor according to claim 16, wherein each of said source regions is annular when viewed from a direction parallel to said side surface of said trench.

18. A transistor comprising:

a semiconductor substrate having a drain layer of a first conductivity type and a conductive region of a second conductivity type formed by diffusing an impurity of the second conductivity type from a surface of said drain layer;

a trench provided such that it extends from a surface of said conductive region to said drain layer;

a source region of the first conductivity type provided inner surface of said conductive region and exposed on a side surface of said trench;

a gate insulating film provided on the side surface of said trench, and an upper part of the gate insulating film being in contact with a lower part of said source region, a bottom part being in contact with an upper part of said drain layer, and a middle part being in contact with said conductive region;

a gate electrode material provided in contact with said gate insulating film in said trench;

a source electrode film provided in contact with said source region exposed at least on the side surface of said trench and electrically insulated from said gate electrode material,

said source region being substantially square when viewed from a direction parallel to said side surface of said trench, wherein the transistor comprises a plurality of said source regions and outer periphery of each said source regions is exposed at a side of upper part

of said trench; and

a metal film formed on a surface of said drain layer opposite to said conductive region to establish Schottky contact with said drain layer.

19. A transistor according to claim 18, wherein each of said source regions is annular when viewed from a direction parallel to said side surface of said trench.